	Type	Hits	Search Text
1	BRS	998	(semiconductor adj wafer) and (temperature same control same gas)and @ad<20000317
2	BRS	75	((semiconductor adj wafer) and (temperature same control same gas)and @ad<20000317) and ((local or localized) with wafer)

	DBs	Time Stamp	Comments	Error Definition
1	USPAT; US-PGPUB	2001/07/02 09:13		
2	USPAT; US-PGPUB	2001/07/02 09:14		

DOCUMENT-IDENTIFIER: US 6123766 A
TITLE: Method and apparatus for achieving temperature uniformity of a substrate

BSPR:
Another way to increase substrate temperature uniformity is to use a temperature-sensitive process such as an oxide growth to grow a test film on a wafer. Oxide growth on silicon occurs at well-characterized rates for varying temperatures. By growing an oxide on silicon for a known amount of time and then measuring the thickness of the grown oxide as a function of the wafer radius using an ellipsometer or profilometer, the **local** temperature of the substrate may be obtained (also as a function of radius). Here, the term "local temperature of the substrate" is used to mean the temperature at a specified small area of the substrate, where "small" refers to a characteristic size over which the temperature variation is minimal.

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A processing region 163 is located generally above substrate 117. In processing region 163, and to a certain extent in other areas of the chamber, process gases are used in conjunction with the **temperature control** of substrate 117 via lamps 110 to conduct chemical reactions on substrate 117. These reactions include, but are not limited to, oxidation or nitridation film growth, etc. The process gases typically enter processing region 163 through a **gas** plenum or showerhead located above or to the side of processing region 163. As shown in FIG. 6, these gases enter via a **gas** inlet 177. If necessary, process gases may be pumped out of the chamber or exhausted by a pumping system 179 of known design. Details of such devices are provided in the U.S. Pat. No. 5,155,336, incorporated by reference above.

DOCUMENT-IDENTIFIER: US 5834068 A
TITLE: Wafer surface temperature control for deposition of thin films

ABPL:
A method for improving the characteristics of deposited thin films by improved **control** and stabilization of wafer surface temperatures. Further, the invention provides the ability to rapidly change the **temperature** of the wafer surface without the need to change the **temperature** of the chamber. The wafer is heated to an operating **temperature** by conventional means. A **gas** with high thermal conductivity, such as helium or hydrogen, is passed over the wafer to cool its surface to a desired **temperature** for the process to be performed. The flow rate is then adjusted to stabilize the **temperature** of the wafer and reduce surface **temperature** variations. Processing gases are then introduced into the chamber, and deposition onto the wafer commences. The maintenance of correct wafer surface **temperature** results in improved step coverage and conformality of the deposited film. Post-deposition steps such as plasma annealing may be performed using a **gas** compatible with the process at a flow rate which results in a **temperature** desirable for the post-deposition process.

DEPR:
In overview, this invention is based on the use of gases with high thermal conductivities such as hydrogen or helium, to reduce or otherwise **control** the surface **temperature** of a wafer shortly before thermal CVD processing. The flow of a cooling **gas** such as hydrogen is used to **control** and stabilize the **temperature** of the wafer surface to maintain it at a **temperature** desired for the process being run. The present invention thus provides for **localized temperature control of the wafer,** with attendant benefits in

reduced transient
time, improved bottom step coverage and conformality of
deposition, and
improved processing results from pre- and post-deposition
processes.

DEPR:
The present invention may be used to provide **localized wafer temperature control,** for whatever reason, in an environment that must remain at an elevated **temperature**. The cooling **gas** and the flow rate may also be changed to accommodate a different process in the same chamber, and thus, multiple consecutive processes may be run in a single chamber at different wafer surface temperatures for each process. Transient time required for wafer transfer to different chambers or to change the **temperature** of the chamber is minimized, and processes are able to be run at optimum temperatures to achieve improved results. Additionally, because multiple processes may be run in a single chamber, the particulate contamination that often attends wafer transfer between chambers is reduced.

DEPR:
After deposition ends and before plasma bombarding of the deposited film begins, the flows and types of gases may be adjusted to allow the **temperature** of the wafer 114 to rise to an optimum **temperature** for the plasma bombarding process. Once the desired wafer surface **temperature** has been reached, the flow of cooling **gas** is adjusted to maintain the wafer 114 at a constant **temperature,** and plasma bombarding commences. During plasma bombarding, a plasma **gas,** such as a combination of nitrogen, hydrogen, argon and other noble gases is supplied to the showerhead 136 by the **gas** panel 52 under **control of the gas** panel controller 50.

DEPR:

In contrast in the process of the invention using gases with higher thermal conductivities to cool wafer surface **temperature,** with He or H.sub.2 in the pre-deposition step and N.sub.2 as the diluent **gas** in the deposition step, even with a 450.degree. C. susceptor **temperature,** where the step coverage is about 70%. If the process is run with H.sub.2 or He as the diluent **gas** in the deposition step, the step coverage is above 80% at a susceptor **temperature** of 450.degree. C. FIG. 6(b) is a table showing the step coverage achieved with various gases and flow rates. As can be seen from the table, the greatest step coverage is achieved with 1600 sccm of hydrogen during the pre-deposition step, and 300 sccm of helium as a carrier **gas** and 100 sccm of hydrogen as a diluent during the deposition. These improvements are due to the ability to hold the **temperature** of the wafer surface at a **temperature** different from the susceptor **temperature**. The high step coverage and highly conformal coverage of the corners between the bottom and walls of the contact/via hole are shown by FIG. 7, which is an SEM (Scanning Electron Microscope) micrograph of a CVD TiNxP film deposited using the wafer surface **temperature control** process of the invention, in which 80% step coverage was achieved.

DOCUMENT-IDENTIFIER: US 5851294 A
TITLE: Gas injection system for semiconductor processing

BSPR:
The nozzles of available gas distribution devices are typically configured to inject the gaseous substances in the general direction of the wafer. As the complexity and packaging density of integrated circuits increases, the uniformity of the film formed on the wafer surface is becoming of greater importance. The rate of film development radially across the wafer surface depends upon such factors as the gas flow rate and the position and orientation of the nozzle relative to **localized** areas of the wafer surface. A gas distribution apparatus in which the nozzles are arranged to produce a substantially uniform layer of film on the wafer surface is desirable.

DEPR:
FIG. 1 shows a **gas** injection assembly 10 which is particularly suitable for delivering a gaseous substance to a chamber 12 of processing system 14. Processing system 14 is used for plasma-enhanced chemical vapor deposition processing, although it is to be understood that the injection assembly 10 may also be used with other processes on the wafer including, but not limited to, chemical vapor deposition, etching, high **temperature** film deposition, and the like. Processing system 14 generally includes a chamber wall 16 and a top plate 18 enclosing the chamber 12. A support assembly 20 supports a wafer 22 within the chamber 12 for processing. In the preferred embodiment, the support assembly 20 is an electrostatic clamp assembly of the type disclosed in co-pending application Ser. No. 08/500,480, the disclosure of which is incorporated herein by reference. However, other types of support systems such

as a mechanical clamping chuck may be used if desired. A plasma source 24 mounted to the top plate 18 and substantially axially aligned with the wafer 22 generates a supply of plasma for enhancing the processing of the wafer 22. Plasma source 24 is described in detail in co-pending application Ser. No. 08/500,493, the disclosure of which is incorporated herein by reference. A vacuum system (not shown) is provided for exhausting the chamber 12. As is known in the art, the vacuum system generally includes a vacuum pump (not shown) which is operatively coupled to the chamber 12 by a port (not shown). As is described in the application Ser. No. 08/500,493, the vacuum pump may be substantially axially aligned with chamber 12 for improved flow **control** of the gases and plasma. Alternatively, the vacuum pump may be positioned to the side of chamber 12 as is known in the art.

DOCUMENT-IDENTIFIER: US 5926742 A
TITLE: Controlling semiconductor structural warpage in rapid thermal processing
by selective and dynamic control of a heating source

BSPR:
Both intrinsic and extrinsic stresses of the wafer, localized in a specific
area or uniformly spread across its topography, impact on the flatness of the
wafer. The wafer level distortion, in the form of a curve or pattern movement,
translates into more stringent critical dimensions and overlay requirements at
the lithography step level.

BSPR:
Yet, regardless of how sophisticated past attempts at maintaining a
semiconductor structure at a uniform temperature during RTP to minimize warpage
may have been, none have proven completely successful. Consequently, the very
act of RTP treatment of a substrate imparts some unavoidable measure of
deformation to the substrate. Further, as mentioned above, such deformation
may be exacerbated by other localized or generalized intrinsic and extrinsic
stresses acting upon the wafer.

BSPR:
RTP and other transient heating methods enable comparatively rapid "ramp up,"
"steady state" and "ramp down" cycling. For instance, ramp up and ramp down
rates may range from about 2.degree. C./min to about 200.degree. C./sec and
steady state treatment temperatures generally range from about 700 to about
1250.degree. C. In accordance with these techniques, intense radiation quickly
brings the semiconductor structure and any growth, deposition or other
treatment gas that may be present adjacent the structure's surface up to an
optimal treatment temperature, usually in a matter of seconds. This treatment

temperature is maintained for as long as needed (typically several seconds) whereupon the radiation is deactivated and the structure cools in a matter of seconds. Because of the brief heating/cooling time cycles it provides, transient heating permits accurate control of the semiconductor fabrication procedures in which it may be used, e.g., deposition, growth, doping, patterning, annealing and other sequences, while conserving the thermal budget of the fabrication process.

BSPR:
The very characteristics which make RTP and related rapid heating systems attractive methods by which to manufacture semiconductor devices also can contribute to undesirable structural deformation of the devices. For example, RTP systems include chamber, lamp and reflector configurations designed to produce intense radiation and rapid ramp rates. Combining these effects with the incoming reactant gases and the intricate patterned structures formed on the semiconductor substrates may result in considerable intrinsic and extrinsic wafer stresses. These stresses, in turn, may manifest themselves as localized or generalized deformities in the wafer's topography.

DOCUMENT-IDENTIFIER: US 6151447 A
TITLE: Rapid thermal processing apparatus for processing semiconductor wafers

ABPL:
A novel rapid thermal process (RTP) reactor processes a multiplicity of wafers or a single large wafer, e.g., 200 mm (8 inches), 250 mm (10 inches), 300 mm (12 inches) diameter wafers, using either a single or dual heat source. The wafers or wafer are mounted on a rotatable susceptor supported by a susceptor support. A susceptor position **control** rotates the wafers during processing and raises and lowers the susceptor to various positions for loading and processing of wafers. A heat controller controls either a single heat source or a dual heat source that heats the wafers to a substantially uniform **temperature** during processing. A **gas** flow controller regulates flow of gases into the reaction chamber. Instead of the second heat source, a passive heat distribution is used, in one embodiment, to achieve a substantially uniform **temperature** throughout the wafers. Further, a novel susceptor is used that includes a silicon carbide cloth enclosed in quartz.

BSPR:
A number of different deposition reactors have been developed. Generally, each deposition reactor has a reaction chamber, a wafer handling system, a heat source and **temperature control, and a gas** delivery system (inlet, exhaust, flow **control**).

DEPR:
FIG. 2A is a simplified cross-sectional view of an RTP reactor 200, according to one embodiment of the invention, for processing a multiplicity of wafers 210. Wafers 210 are mounted on a susceptor 201 supported by susceptor support

212. Susceptor position **control** 202 rotates wafers 210 during processing and
raises and lowers susceptor 201 to various positions for loading and processing
of wafers 210. Heat **control** 203 controls a single heat source 204 that heats
wafers 210 to a substantially uniform **temperature** during processing. **Gas** flow
control 205 regulates flow of gases into reaction chamber 209 of reactor 200
through inlet channel 206 and **gas** injection head 207 and exhausts gases from
reaction chamber 209 through outlet channel 208.

DEPR:
As noted above, susceptor 402 can be rotated. Susceptor 402 can be rotated in
either the clockwise or counterclockwise directions. The rotation of susceptor
402 causes the position of each point on the surface of wafer 511 (excepting a
point coincident with the axis of rotation of susceptor 402) to continually
vary, relative to the mean direction of gas flow past wafer 511, during
operation of reactor 400. Consequently, the effect of non-uniformities in
heating or gas distribution that would otherwise create non-uniformities in a
film deposited on wafer 511, as well as dislocations and slip on wafer 511, are
substantially negated. The rotation distributes the non-uniformities in
heating or gas distribution over the upper surface 511a of wafer 511 (FIG. 5F)
rather than allowing them to be **localized** at a particular spot. Typically,
susceptor 402 is rotated at a speed of 0.5-30 rpm. The exact speed is
determined empirically as part of the process of "tuning" reactor 400 after
reactor 400 has been designated for a particular application.

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temperature is maintained for as long as needed (typically several seconds) whereupon the radiation is deactivated and the structure cools in a matter of seconds. Because of the brief heating/cooling time cycles it provides, transient heating permits accurate **control** of the semiconductor fabrication procedures in which it may be used, e.g., deposition, growth, doping, patterning, annealing and other sequences, while conserving the thermal budget of the fabrication process.

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The very characteristics which make RTP and related rapid heating systems attractive methods by which to manufacture semiconductor devices also can contribute to undesirable structural deformation of the devices. For example, RTP systems include chamber, lamp and reflector configurations designed to produce intense radiation and rapid ramp rates. Combining these effects with the incoming reactant gases and the intricate patterned structures formed on the semiconductor substrates may result in considerable intrinsic and extrinsic wafer stresses. These stresses, in turn, may manifest themselves as **localized** or generalized deformities in the wafer's topography.

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